10/707,774 Specification Amendments.

1. Please amend paragraph [0001] as follows:

[0001] This patent application is a continuation in part application of a provisional patent application serial number 60/319,085 filed January 22, 2002 entitled "Gate Drive Method for Fast Turn-Off of MOSFETs" ,a provisional patent application serial number 60/429,990 filed November 30, 2002, entitled "Gate Drive Method and Apparatus for the Fast Switching of MOSFETs", and a patent application serial number 10/248,438 filed [[.]]20 January, 2003, entitled "Gate Drive Method and Apparatus for Reducing Losses in the Switching of MOSFETs".

[Note: a period "." was added at the end.]

2. Please amend paragraph [0016] as follows:

[0016] Figure 3.1 shows that the Miller effect is greatly reduced if the gate current is greater than the drain current (low resistance from gate to source).

Figure 4 shows the addition of a capacitor from the drain to the source.

[Note: a period "." was added after "--source)". A new paragraph was started with "Figure 4 ---".

3. Please amend paragraph [0046] as follows:

[0046] Figure 2 shows the familiar gate characteristics during turn off, as described above and as often shown in MOSFET application notes. Turn off is initiated by reducing the gate voltage V_{gs} as shown. At first, from t_0 to t_1, the gate voltage V_{gs} decreases. This is the region where the gate voltage V_{gs} is more than is needed to sustain the drain current i_d. When the gate voltage V_{gs} drops sufficiently so that the MOSFET 3 begins to "pinch off", the channel resistance will begin to rise, and so will the drain voltage V_{ds}. Once the drain voltage V_{ds} begins to rise, a current will flow through the drain-gate capacitance 11. An equilibrium will be reached when the current through the drain-gate capacitance 11 equals the gate current i_g, and the gate voltage V_{gs} will remain constant as the drain voltage V_{ds} rises. During this time period, t_1 to t_2, the full load current I_d continues to flow into the drain 19. When the drain voltage V_{ds} reaches its final value, there will no longer be a Miller current through the gate-drain capacitance 11, and the gate voltage V_{gs} will once again fall. As it does, so will the drain current I_d, from t_2 to t_3, governed by the transconductance characteristics of the MOSFET 3, as would be well known to one skilled in power converter design. At t_3, the threshold voltage is reached, and "pinch off" is complete. The gate voltage continues to discharge past t_3 to zero.

Figure 3 shows that if the gate current i_g exceeds the drain current i_d, then the gate capacitance will continue to discharge in the time period ~~form t_2~~

from t_2 to t_3, V_{gs} will continue to fall, and the "Miller shelf" will be absent. This is because, as explained above, the drain current i_d is the upper limit of the Miller current. If the gate current i_g exceeds the Miller current, then the gate capacitance will discharge and the gate voltage V_{gs} must fall. In figure 3, the gate current i_g is shown as if it were from an ideal switched current source. The I_d shown is the current through the channel.

[Note: a period "." was added after "--zero)". A new paragraph was started with "Figure 3 ---".].

4. Please amend paragraph [0047] as follows:

[0047] As an aside, when trying to model the above behavior using available SPICE MOSFET models, even with a short circuited gate the crossover voltage and current characteristics were present. It seems that commercially available MOSFETs have too high a gate mesh resistance for the effect to be seen. Although it could not be seen at the gate terminal of the SPICE MOSFET models, the Miller shelf was present internally. The only way to show the teachings of this invention using available SPICE MOSFET models was to use a switched constant current source in the SPICE model on the gate, with the current source set to be larger than the drain current. Then the I_d and V_{ds} curves of figure 3 could be seen.[[.]] A custom SPICE MOSFET model having a low gate mesh resistance had to be made and used to show the teachings of the

invention. This showed convincingly that a new MOSFET design having a low gate mesh resistance would have to be made to use this invention.

5. Please amend paragraph [0048] as follows:

[0048] In a gate drive of this invention, the gate drive for turn off will be a low resistance from the gate to the source, such as a turned on second MOSFET or plurality of MOSFETs. If the gate resistance is sufficiently low, Ig will be greater than I_d, and the graph will be as shown in figure 3.1. There will be a Miller shelf of sorts, not caused by an equilibrium as in the classical Miller effect, but rather after t_2, and it is the voltage drop across the gate drive resistance as the drain voltage is rising as the drain current charges the drain to gate capacitance 11. If designed in according with the teachings of this invention, this pseudo-Miller shelf will occur well below the cut-off gate voltage Vth so that there will be no lossy conduction through the channel during this time, ~~t_x to t_y~~ t_2 to t_3. The I_d shown is the current through the channel. The voltage of the pseudo-Miller shelf will be I_g times the resistance of the gate drive circuit (the driver resistance plus the gate mesh resistance of the MOSFET being switched and any other circuit loop resistances).

6. Please amend paragraph [0059] as follows:

[0059] Commercially available MOSFETs for power converter applications are not well suited for very fast, high current gate drive. The lead and package inductances are much too high, as is the gate mesh resistance.

Of particular concern is the gate mesh resistance, shown ~~lump[ed~~ lumped into the resistance 47 in figure 6. Not only does the gate mesh resistance limit the gate current, it also forms a distributed RC-RC-RC circuit to the various cells of the MOSFET, and there can be significant delay to the cells that are most remote from the gate metalization.

7. Please amend paragraph [0070] as follows:

Figure 6.7 shows how a MOSFET die of this invention might be constructed, as an illustration, not a limitation. A MOSFET die 671 has a drain connection 673 that is the bottom surface of the MOSFET die 671. The top surface 679 of the MOSFET die 671 may have a source connection 675 and a gate connection 677, and the active region 679 of the MOSFET comprises a large number of MOSFET cells 681-681. Each of the MOSFET cells 681-681 can be represented as a MOSFET 683-683. Distributed among the MOSFET cells 681-681 are specialized gate turn off driver cells 691 for turning off the MOSFETs 683-683. As shown in figure 6.8, with reference to figures 6.6 and 6.7, the gate mesh for the MOSFETs 683-683 is represented by a plurality of resistors 687-687 connecting the gates 685-685 of the MOSFETs 683-683 to the gate connection 675. At numerous nodes throughout the MOSFET die 671, the specialized gate turn off drivers 691 connect the gate mesh to the source metalization S. The driver cells 691 are turned on by a common gate turn off drive connection ~~693~~ 893.

8. Please amend paragraph [0083] as follows:

[0083] Typically, in a MOSFET, the Rds is very low in the ON state, and will have millivolts of forward drop at the rated current. In this invention, the gate drive must carry an even larger current, and the question arises about just how low its impedance must be. It must be low, but it can be significantly higher than the Rds of the MOSFET. Whereas the MOSFET will have a voltage drop in millivolts, the gate drive can have higher voltage drop. So, even if it is carrying a current that is larger than the drain current, it may still have a larger resistance. For one, the current is pulsed and has a very short duration. For another, it can have a drop of several tenths of a volt, (or even a volt or more for a MOSFET with a high cutoff threshold) and still pull the gate down with sufficient current. Further, the MOSFET being switched may be a higher voltage device and ~~ay~~ may have to withhold a high voltage, but the gate drive will have a voltage that is comparatively very low. Thus the silicon area needed for the gate drive pull-down MOSFET can be small compared to silicon area of the MOSFET[[.]] being switched.

9. Please amend [0084] as follows. The conditions recited in [0084], amplified and explained further by the discussion in the paragraphs preceding [0084], are stated in the form of a definition to support language in the specification and the claims. No new matter has been added.

[0084] More specifically, with a MOSFET being switched that is designed for a maximum drain current I_d, and a gate pinch off threshold voltage of V_{th}, the resistance of the turn off driver circuit must be less than a resistance equal to V_{th}/I_d. This is the marginal case, and preferably the resistance is much less than V_{th}/I_d. For the case with a parallel capacitor C_p, this resistance can be larger, by a factor of $(C_p + C_{dg})/C_{dg}$. In this specification and the claims, a recitation that the gate of a first MOSFET is characterized by having a very low gate resistance; the on resistance of the a second MOSFET is characterized by having a very low channel resistance; the source connection has a very low impedance; and the drain-gate connection has a very low impedance so that when the MOSFET is turned on, a gate current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET so that the gate current i_g is larger than the load current i_d means that sum of the respective resistances and impedances is sufficiently low so that the sum of the respective resistances and impedances is less than the ratio V_{th}/I_d.